Hritom Das — Assistant Professor

CONTACT INFORMATION: Oklahoma State University
ECE Department, 265 Engineering South,
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EDUCATION:

Ph.D. in Electrical and Computer Engineering, North Dakota State University, Fargo, ND, USA **(Fall-2020)**

GPA- 3.86/4.0
Advisors: Dr. Na Gong and Dr. Scott C. Smith
Dissertation Topic: Power-Efficient Adaptive Memory Design and Optimization for Videos and Deep Learning

MSc in Electronic Engineering, KNU, Daegu, South Korea **(Fall-2015)**
GPA – 3.71/4.30
Advisor: Dr. Yeonbae Chung
MSc. Thesis Title: Data Retention Characteristics of NMOS-Style 2T Gain Cell DRAM.

BSc in Electrical & Electronic Engineering, AIUB, Dhaka, Bangladesh. **(Fall-2012)**
GPA – 3.65/4.0
Advisor: Mr. Subrata Biswas
BSc. Thesis Title: A Novel Design and Performance Evaluation of CNTFET Subtractor Cell Using Fine Grain Sleep Transistor for Nano Electronics.

PROFESSIONAL EXPERIENCE:

- Assistant Professor **Fall-2024→ Present**
  Oklahoma State University
  Electrical Engineering and Computer Engineering
  265 Engineering South,
  Stillwater, OK 74078, USA

- Post-Doctoral Research Associate **Spring-2022→ Summer 2024**
  Advisor: Dr. Garrett S. Rose
  The University of Tennessee
  Electrical Engineering and Computer Engineering
  Knoxville, TN 37996-2250, USA

- Post-Doctoral Research Associate **Spring-2021→ Fall 2021**
  Advisor: Dr. Na. Gong
  University of South Alabama
  Electrical & Computer Engineering
  Mobile-36688, AL 36688, USA.

- Assistant Professor (Adjunct) **Spring-2021→ Fall-2021**
  University of South Alabama
  Electrical & Computer Engineering
  Mobile-36688, AL 36688, USA.

AWARDS AND HONORS:

1. Brain Korea-21(BK-21) Honors. **(Spring-2014 → Fall-2014)**
2. Kyungpook Honors Scholarship (KHS) **(Spring-2015 → Fall-2015)**

TEACHING INTEREST:

Emerging Devices, Neuromorphic Circuit and System**,** Fault Tolerant System Design and Analysis, Approximate Computation, Data Storage and Transmission with Privacy, Digital System Design, Advanced Digital Design, Embedded Systems, Computer Organization, VLSI, Microprocessor System Design, Electronics, and Circuit Theory.

TEACHING EXPERIENCE:

- **Courses Taught as Adjunct Faculty in University of South Alabama: Spring-2021→ Fall-2021**
  I. Microprocessors Systems & Interfacing (Lecture + Lab) II. Digital Logic Design (Lecture + Lab)
- **Guest Lecturer in North Dakota State University Fall-2018→Fall-2020**
  I. Digital Design (ECE 275) II. VLSI Design (ECE 623)
- **Teaching Assistant in North Dakota State University** (**Fall-2017→Fall-2020**)
  I. Digital Design (ECE 275) II. Electronics 1 (ECE 321) III. Computer Organization (ECE 374)
- **Lecturer, Uttara University, Dhaka, Bangladesh**. **(Fall-2016→Spring-2017)**
  I. Digital Design II. Electronics 1 & 2 III. VLSI

RESEARCH INTEREST:

- Investigate emerging devices based on different materials (e.g. HfO2, NbO2).
- Neuromorphic circuit & system design and analysis.
- Low power learning circuit (e.g. STDP, Homeostatic plasticity) design for a dynamic environment.
- Circuit and system (e.g. synapse, neuron, STDP) modeling to predict the behavior of it in complex dynamics.
- Framework development & testing with different applications to evaluate the performance of our design.
- Smart and tiny processor (e.g. DPE) design for edge computation (smart camera).
- Differential privacy for edge devices.
- Hybrid memory (e.g. conventional + emerging, volatile + nonvolatile) design to meet the performance requirement.
- Conventional Memory (SRAM, DRAM) design and testing for video data and image processing.
- Ultra-low power IC design for longer battery life for mobile devices.

RESEARCH PROPOSAL WRITING EXPERIENCE:

- **Title:** Neuromorphic Materials and System Integration for Extreme Environments
  - **Funding Opportunity Number:** FOA-AFRL-AFOSR-2023-0012
  - **Opportunity Title:** CENTER OF EXCELLENCE (COE): Extreme Neuromorphic Materials and Computing
- **Title:** EMERGING MATERIALS, DEVICES AND TECHNOLOGIES FOR EDGE AI
  - **Funding Opportunity:** Northeast Regional Defense Technology Hub (NORDTECH)
  - **Opportunity Title:** EMERGING MATERIALS to SYSTEM for EFFICIENT AI DEPLOYMENT
- **Title:** Cross-layer Co-design of Threshold Switch-Assisted Hybrid Memory Systems
  - **Program Title:** NSF 23-552
  - **Opportunity Title:** Future of Semiconductors (FuSe)
- **Title:** Development of a Cross-layer Electronic Characterization Platform for Emerging Nanoelectronics
  - **Funding Opportunity:** NSF 23-519
  - **Opportunity Title:** Major Research Instrumentation (MRI) Program
- **Title: Efficient Learning of Spatiotemporal Regularities in Humans and Machines through Temporal Scaffolding**
  - **Funding Opportunity:** NSF 21-615
    - **Opportunity Title:** Emerging Frontiers in Research and Innovation

RESEARCH EXPERIENCE:

- **Post-Doctoral Research Associate**, **SENECA Lab** (**Spring-2022→present)**

Location: University of Tennessee, Knoxville, Department of Electrical Engineering & Computer Science
Duties:

- Design and optimize memristive (HfO2) synapses to evaluate their performance at extreme conditions such as at low or high temperatures with a cryogenic probe station.
- I am developing synaptic DPE, STDP, and Homeostatic plasticity circuitry for neuromorphic systems.
- I was involved in developing an in-house SRAM compiler, which is compatible with any CMOS technology.

- This spring, I was involved with a full chip tape-out 5mm x 6mm. There were 7 clusters, with 32 neurons in each cluster. This is a memristive design with two networking layers (R1 & R2). Moreover, RISC V was there to communicate with the memristive core by AXI lite.
- I am also mentoring graduate students (Ph.D. and M.Sc.) to complete their research tasks and helping them to write research papers.
- Moreover, I am helping my supervisor to write proposals.

(Funded by: FA8750- 21-1-1018)
Awarded amount: $2,015,194.00

- **Post-Doctoral Research Associate, IMPACT Lab** (**Spring-2021→Fall- 2021)**

Location: The University of South Alabama, Department of Electrical and Computer Engineering
Duties:
- Low-powered and secured (differential private deep learning, data privacy) circuit design (SRAM, DRAM) for video technology.
- ECC adaptation to optimize power, performance, and area of the system.

(Funded by NSF: CCF-1855706)
Awarded amount: $316,000.00.

- **Graduate Research Assistant**, **IMPACT Lab** **(Summer-2017→Fall- 2020)**

Location: North Dakota State University, Electrical and Computer Engineering
Duties:
- Mathematical Models for Optimal Video Memory Design
- Memory Optimization for Energy-Efficient Differentially Private Deep Learning
- Flexible Low-Cost Power-Efficient Video Memory with ECC-Adaptation
- Secure Data Transmission and Error Correction with ECC Adaptive SRAM

(Funded by: NSF CCF-1855706)
Awarded amount: $316,000.00

- **Graduate Research Assistant, ULSI Lab** **(Spring-2014→Fall-2015)**

Location: Dept. of Electrical & Comp. Eng., Kyungpook National University. S. Korea
Duty:
- Characterization and retention time enhancement of 2T DRAM

(**Funded** by Samsung R&D, Memory Division (South Korea) and National Research Foundation of Korea **(NRF-2014R1A1A4A01008225)**

- **PUBLICATIONS**

JOURNAL PAPERS CURRENTLY UNDER REVIEW:

7. **H. Das**, et al., "Enhanced Read Resolution in Reconfigurable Memristive Synapses for Spiking Neural Networks," ***Nature Communication*** (2024).
6. M. Rathore, **H. Das**, M. Liehr, G. S. Rose, N. Cady, "Comprehensive Empirical Model for Variability and Failure Analysis of HfO2 Memristors," ***IOP Science*** (2023).
5. N. N. Chakraborty, **H. Das**, C. D. Schuman, G. S. Rose, "A Reconfigurable Neuron Design to Enhance the Performance of Neuromorphic Applications," ***Nature Communication*** (2023).
4. N. N. Chakraborty, S. O. Ameli, **H. Das**, C. D. Schuman, G. S. Rose, "Hardware-Software Co-design by Leveraging Spike-Timing-Dependent Plasticity in a Memristive NeuroProcessor," ***IOP Science*** (2023).
3. **H. Das,** et al., "Current Controlled Memristive Synapse for Stochastic Computing in Neuromorphic System," ***Nature Communication*** (2023).
2. SH. Alam, **H. Das**, and G. S. Rose "A Survey of Neuromorphic Computing in Robotics and Relevant Applications," ***IEEE Access*** (2023).
1. J. Lui, N. Gong, and **H. Das** "Two Birds with One Stone: Differential Privacy by Low-power SRAM Memory," ***IEEE Transactions on Dependable and Secure Computing*** (2023).

JOURNAL PUBLICATIONS:

11. **H. Das** et al., "An Efficient and Accurate Memristive Memory for Array-Based Spiking Neural Networks," in ***IEEE Transactions on Circuits and Systems I: Regular Papers***, (Early Access 2023)
10. **H. Das**, R. D. Febbo, C. P. Rizzo, N. N. Chakraborty, J. S. Plank and G. S. Rose, "Optimizations for a Current-Controlled Memristor-based Neuromorphic Synapse Design," in ***IEEE Journal on Emerging and Selected Topics in Circuits and Systems***, (Early Access 2023)

9. **H. Das**, A. A. Haidous, S. C. Smith and N. Gong, "Approximate Memory for Low-Power Video Applications," in ***IEEE Access***, vol. 11, pp. 57735-57744, 2023
8. A. Haidous, W. Oswald, **H. Das,** and N. Gong, "Content-Adaptable ROI-Aware Video Storage for Power-Quality Scalable Mobile Streaming," in ***IEEE Access***, vol. 10, pp. 26830-26848, 2022
7. **H. Das**, A. A. Haidous, S. C. Smith and N. Gong, "Flexible Low-Cost Power-Efficient Video Memory With ECC-Adaptation," in ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems***, vol. 29, no. 10, pp. 1693-1706, Oct. 2021
6. Y. Xu, **H. Das,** and N. Gong, "Application-Aware Quality-Energy Optimization: Mathematical Models Enabled Simultaneous Quality and Energy-Sensitive Optimal Memory Design," in ***IEEE Transactions on Sustainable Computing***, vol. 6, no. 4, pp. 559-571, 1 Oct.-Dec. 2021
5. J. Edstrom, **H. Das**, Y. Xu, N. Gong, "Memory Optimization for Energy-Efficient Differentially Private Deep Learning," ***IEEE Transactions on Very Large-Scale Integration (VLSI) Systems***, Volume: 28, Issue: 2, Feb. 2020.
4. Y. Xu*, **H. Das***, Y. Gong, N. Gong "On Mathematical Models of Optimal Video Memory Design," ***IEEE Transactions on Circuits and Systems for Video Technology***, Volume: 30, Issue: 1, Jan. 2020. (*Equal Contribution)
3. W. Cheng, **H. Das**, and Y. Chung, "A Logic-Compatible Embedded DRAM Utilizing Common-Body Toggled Capacitive Cross-Talk," ***Journal of Semiconductor Technology and Science (JSTS)***, Vol.16, No.6, pp-781-792, December 2016
2. Y. Chung, W. Cheng and **H. Das**, "Built-in parasitic-diode-based charge injection technique enhancing data retention of gain cell DRAM," ***IET Electronics Letters***, Vol. 51, No. 23, pp. 1854-1855, November 5, 2015.
1. D. Das, M. S. Shbat, **H. Das**, V. Tuzlukov, "Diversity Combining techniques under Employment of Generalized Receiver in Communication Systems with Rayleigh Fading Channels," ***Journal of Modern Science and Technology***, Vol. 1, No. 1, pp. 96-112, May 2013.

CONFERENCE PAPERS CURRENTLY UNDER REVIEW:

2. **H. Das** et al., "Low-Power and Optimized Neuromorphic Oscillator Design to Process Sensory Data" In ***2024 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)***
1. **H. Das** et al., "Performance Evaluation of a Memristive Core by Injecting Analog Current," In ***2024 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)***

CONFERENCE PUBLICATIONS:

16. S. H. Alam, **H. Das**, and G. S. Rose, "On-Chip Encoder to Program a Memristor-Based Synaptic Array," In ***2024 IEEE International Symposium on Circuits and Systems (ISCAS) (Accepted)***
15. SNB. Tushar, **H. Das**, and G. S. Rose, "Hfo2 Based Synapse Based Spiking Neural Network Modeling to Optimize the Hardware Design and Testing Cost," In ***2024 IEEE International Symposium on Circuits and Systems (ISCAS) (Accepted)***
14. C. Schuman, **H. Das**, J. Plank, A. Aziz, and G. S. Rose, "Evaluating Neuron Models through Application-Hardware Co-Design," In ***2023 57th Asilomar Conference on Signals, Systems, and Computers. (Accepted)***
13. N. N. Chakraborty, **H. Das**, and G. S. Rose, "Homeostatic Plasticity in a Leaky Integrate and Fire Neuron using Tunable Leak," In 2023 ***IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS)*** 2023 **(Nominated as best paper)**
12. N. N. Chakraborty, **H. Das**, and G. S. Rose. 2023. "Spike-Timing-Dependent Plasticity for a Hafnium-Oxide Memristive Synapse," In 2023 ***IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS)*** *2023*
11. N. N. Chakraborty, **H. Das**, and G. S. Rose. 2023. "Energy Efficient and High-Performance Synaptic Operating Point Evaluation for SNN Applications," In 2023 ***IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS)*** *2023*
10. N. N. Chakraborty, **H. Das**, and G. S. Rose, "Spike-Driven Synaptic Plasticity for a Memristive Neuromorphic Core," In 2023 ***IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS)*** *2023*
9. **H. Das**, M. Rathore, R. Febbo, M. Liehr, N. C. Cady, and G. S. Rose, "Rfam: Reset-failure-aware-model for hfo2-based memristor to enhance the reliability of neuromorphic design," In Proceedings of the ***Great Lakes Symposium on VLSI 2023***, pp. 281-286. 2023.
8. N. N. Chakraborty, **H. Das**, and G. S. Rose, "A Mixed-Signal Short-Term Plasticity Implementation for a Current-Controlled Memristive Synapse," In Proceedings of the ***Great Lakes Symposium on VLSI 2023***, pp. 179-182. 2023

7. M. Rathore, R. Febbo, A. Foshie, S. N. B. Tushar, **H. Das**, and G. S. Rose, "Reliability Analysis of Memristive Reservoir Computing Architecture," In Proceedings of the ***Great Lakes Symposium on VLSI 2023***, pp. 131-136. 2023.
6. R. Weiss, **H. Das**, N. N. Chakraborty, and G. S. Rose, "STDP based online learning for a current-controlled memristive synapse," In 2022 ***IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS),*** pp. 1-4. IEEE, 2022.
5. A. Z. Foshie, C. Rizzo, **H. Das**, C. Zheng, J. S. Plank, and G. S. Rose, "Benchmark Comparisons of Spike-based Reconfigurable Neuroprocessor Architectures for Control Applications," In Proceedings of the ***Great Lakes Symposium on VLSI 2022,*** pp. 383-386. 2022
4. J. Edstrom, **H. Das**, Y. Xu, N. Gong, "Embedded sensory data memory optimization for IoT edge inference with privacy, accuracy, and energy efficiency," ***4th ACM/IEEE Symposium on Edge Computing***, pp.357, November 2019. [Presentation]
3. **H. Das**, Y. Gong, Y. Xu, J. Wang, and N. Gong, "Analytical-Optimization-Model-Driven Energy-Quality Adaptive Memory Framework for Big Video Applications," ***in Proc. 2018 GOMACTech***, pp.935-938, March 2018.
2. **H. Das**, S. Manisankar, W. Cheng, and Y. Chung, "Experimental n-style two-transistor eDRAM in logic CMOS technology," ***in Proc. 2015 IEEE International Conference on Electron Devices and Solid-State Circuits***, pp.75-78, June 2015.
1. W. Cheng, **H. Das**, H. Zheng, B. Zhou, and Y. Chung, "A gain cell based embedded DRAM with fully-restoring write-back scheme," ***in Proc. 2014 International SoC Design Conference***, pp.116-117, November 2014.

POSTER PRESENTATIONS:

2. W. Cheng, **H. Das**, S. Manisankar, and Y. Chung "A Gain Cell eDRAM in Logic CMOS Technology," ***International SoC Design Conference 2015***, South Korea.
1. S. Biswas, T. Islam, **H. Das** "A Novel Design and Performance Evaluation of CNTFET Subtractor Cell for Nanoelectronics," ***International Workshop on Nanotechnology***, 21-23 September 2012, Dhaka, Bangladesh.

REVIEWER:

- IEEE Transactions on Circuits and Systems for Video Technology
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems
- IEEE Transactions on Circuits and Systems I: Regular Papers
- IEEE Transactions on Very Large Scale Integration (VLSI) Systems
- Journal of Circuits, Systems, and Computers
- ICONS, GLSVLSI, ISCAS, MWSCAS, DCAS, ISVLSI, ISQED, ICRC.

TECHNICAL SKILLS:

Programming Languages: VHDL, Verilog, Verilog-A, Skill, Python, C.
Application Tools & Software: Cadence Virtuoso, Caliber (DRC, LVS), Design Compiler, Innovus, Quartus II, ModelSim, MultiSim, HSPICE, PSPICE, MATLAB.
Hardware Packages: FPGA (ALTERA DE2 series, Xilinx), Embedded board (Arduino Uno 328).
Apparatus: Cryogenic probe station, NI PXIe, Pulse/pattern generator, DC power analyzer, Data generator, Variable output pod, Digital phosphor oscilloscope, DigiCAM II, Digital drying oven for high-temperature measurement.

MEMBERSHIP:

- IEEE Member
- IEEE CAS Member
- IEB (The Institution of Engineers, Bangladesh)

SOCIAL LINK:

Google Scholar: https://scholar.google.com/citations?user=EP6x7-8AAAAJ&hl=en
LinkedIn: https://www.linkedin.com/in/hritom-das/
Research Gate: https://www.researchgate.net/profile/Hritom_Das

REFERENCES:

Dr. Garrett S. Rose Professor & Associate Department Head Min H. Kao Department of Electrical Engineering and Computer Science The University of Tennessee 319 Min H. Kao Building Knoxville, TN 37996-2250 USA Phone: 865-974-3132 Email: garose@utk.edu	**Dr. Na Gong** W. Nicholson Professor Department of Electrical and Computer Engineering The University of South Alabama 150 Jaguar Drive, Shelby Hall 4122, Mobile, AL 36688 Phone: 251-460-7683 Email: nagong@southalabama.edu	**Dr. Scott C. Smith** Chair and Professor (Retd.) Department of Electrical Engineering and Computer Science Texas A&M University - Kingsville 700 University Blvd, Kingsville, TX 78363 Phone: 314-681-1504 Email: outdoorsman.smith74@gmail.com
Dr. Catherine Schuman Assistant Professor Min H. Kao Department of Electrical Engineering and Computer Science The University of Tennessee 321 Min H. Kao Building Knoxville, TN 37996-2250 USA Phone: 865-974- 4393 Email: cschuman@utk.edu	**Dr. James S. Plank** Professor Min H. Kao Department of Electrical Engineering and Computer Science The University of Tennessee 320 Min H. Kao Building Knoxville, TN 37996-2250 USA Phone: 865-974-4397 Email: jplank@utk.edu	**Dr. Nathaniel C. Cady** Empire Innovation Professor Associate Dean for Research Executive Director – SUNY Applied Materials Research Institute (SAMRI) University at Albany, SUNY 4405 NanoFab East 257 Fuller Road, Albany, NY 12203 Phone: 518-956-7354 Email: ncady@albany.edu